1. A method of forming at least one contact in a magnetic random access memory cell structure, said method comprising:

forming a plurality of first conductive layers in an insulating layer of a substrate;

forming a plurality of first magnetic layers over said respective first conductive layers;

forming a plurality of second magnetic layers spaced along said first magnetic layers;

forming an insulating material in between and over said first and second magnetic layers; and

removing portion of said insulating material to expose at least one upper surface of a conductive layer, said conductive layer being part of said second magnetic layer.

2. The method of claim 1, wherein said act of removing portion of said insulating material further comprises exposing a plurality of upper surfaces of conductive layers respectively associated with said second magnetic layers.

3. The method of claim 1 further comprising forming nonmagnetic layers between said second magnetic layers and said first magnetic layers.

4. The method of claim 2, further comprising forming a plurality of second conductors each in electrical connection with a plurality of said exposed upper surfaces

of said conductive layers, said plurality of second conductors running substantially orthogonal to said conductive layers.

5. The method of claim 1, wherein said act of removing portion of said insulating material further comprises chemical mechanical polishing of said insulating material to expose said upper surface of said conductive layer.

6. The method of claim 1, wherein said conductive layer is formed of a material selected from the group consisting of tungsten nitrogen, tungsten, gold, platinum and copper.

7. The method of claim 1, wherein said insulating material is formed of a material selected from the group consisting of silicon nitride and oxides.

8. The method of claim 1, wherein said insulating material is a high temperature polymer.

9. The method of claim 1, wherein said insulating material is a low dielectric constant inorganic material.

10. The method of claim 1, wherein said insulating material is silicon nitride.

11. The method of claim 1, wherein said act of forming said first magnetic layers further comprises the step of forming a first plurality of stacked layers, said first plurality of stacked layers including at least one magnetic material layer.

12. The method of claim 11, wherein said magnetic material layer contains a material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

13. The method of claim 12, wherein said first plurality of stacked layers comprises layers of tantalum, nickel-iron and manganese-iron.

14. The method of claim 12 further comprising etching said first plurality of stacked layers to have a width which coincides with the width of said first conductive layers.

15. The method of claim 1, wherein said act of forming said second magnetic layers further comprises forming a second plurality of stacked layers, said second plurality of stacked layers including at least one magnetic material layer and said conductive layer.

16. The method of claim 15, wherein said magnetic material layer includes a material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

17. The method of claim 16, wherein said second plurality of stacked layers comprises layers of tantalum, nickel-iron and tungsten nitrogen.

18. The method of claim 16, further comprising etching said second plurality of stacked layers.

19. The method of claim 1, wherein said first magnetic layers have a pinned magnetic orientation.

20. The method of claim 1, wherein said second magnetic layers have a free magnetic orientation.

21. A method of forming a plurality of self-aligned contacts of respective magnetic random access memory cells formed over a semiconductor substrate, said method comprising:

forming a plurality of first conductive layers in an insulating layer formed over said semiconductor substrate;

forming a plurality of first magnetic layers over respective first conductive layers;

forming a plurality of second magnetic layers spaced along said first magnetic layers, said plurality of second magnetic layers including respective top conductive layers;

forming an insulating material over said substrate and said plurality of first and second magnetic layers including said top conductive layers, and in between adjacent first and second magnetic layers;

removing portions of said insulating material from said top conductive layers to expose a plurality of upper surfaces of said top conductive layers associated with said second magnetic layers; and

forming a plurality of second conductive layers over respective self-aligned contacts, said second conductive layers running substantially orthogonal to said first magnetic layers; one of said first and second conductive layers being bit lines and the other of said first and second conductive layers being word lines.

22. The method of claim 21, further comprising forming a plurality of nonmagnetic layers between said plurality of second magnetic layers and said plurality of first magnetic layers.

23. The method of claim 22, wherein said nonmagnetic layers are formed of a material selected from the group consisting of aluminum oxide, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

24. The method of claim 21, wherein said act of forming said insulating material further comprises depositing said insulating material.

25. The method of claim 21, wherein said act of removing portion of said insulating material further comprises chemical mechanical polishing of said insulating material relative to said upper surfaces of said top conductive layers.

26. The method of claim 21, wherein said top conductive layers are formed of a material selected from the group consisting of tungsten nitride, tungsten, gold, platinum and copper.

27. The method of claim 21, wherein at least one of said top conductive layers is formed of tungsten nitride.

28. The method of claim 21, wherein at least one of said top conductive layers is formed of tungsten.

29. The method of claim 21, wherein said insulating material is formed of a material selected from the group consisting of silicon nitride and oxides.

30. The method of claim 21, wherein said insulating material is a high temperature polymer.

31. The method of claim 21, wherein said insulating material is a low dielectric constant inorganic material.

32. The method of claim 21, wherein said insulating material is silicon nitride.

33. The method of claim 21, wherein said act of forming said plurality of first magnetic layers further comprises the step of forming a first plurality of stacked layers, said first plurality of stacked layers including at least one magnetic material layer.

34. The method of claim 33, wherein said magnetic material layer contains a material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

35. The method of claim 34, wherein said first plurality of stacked layers comprises layers of tantalum, nickel-iron and manganese-iron.

36. The method of claim 34 further comprising etching said first plurality of stacked layers to have a width which coincides with the width of said plurality of first conductive layers.

37. The method of claim 21, wherein said act of forming said plurality of second magnetic layers further comprises forming a second plurality of stacked layers, said second plurality of stacked layers including at least one magnetic material layer and said top conductive layer.

38. The method of claim 37, wherein said magnetic material layer includes a material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

39. The method of claim 38, wherein said second plurality of stacked layers comprises layers of tantalum, nickel-iron and tungsten nitrogen.

40. The method of claim 39 further comprising etching said second plurality of stacked layers.

41. The method of claim 21, wherein said first magnetic layers have a pinned magnetic orientation.

42. The method of claim 21, wherein said second magnetic layers have a free magnetic orientation.

43. A magnetic random access memory structure comprising:

a plurality of longitudinally extending conductive first lines formed over an insulating layer of a semiconductor substrate;

respective first magnetic layers over said conductive first lines;

respective spaced apart second magnetic layers over said first magnetic layers; and

at least one self-aligned contact formed of a conductive layer of said at least one spaced apart second magnetic layer.

44. The magnetic random access memory structure of claim 43, further comprising a nonmagnetic layer between said first magnetic layers and said second magnetic layers.

45. The magnetic random access memory structure of claim 44, wherein said nonmagnetic layer comprises a material selected from the group consisting of aluminum oxide, titanium oxide, magnesium oxide, silicon oxide and aluminum nitride.

46. The magnetic random access memory structure of claim 43, wherein said conductive layer is formed of a material selected from the group consisting of tungsten, tungsten nitrogen, copper, gold and platinum.

47. The magnetic random access memory structure of claim 43, wherein each said first magnetic layer includes a magnetic material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

48. The magnetic random access memory structure of claim 43, wherein each said second magnetic layer includes a ferromagnetic material selected from the group consisting of tantalum, nickel-iron, tungsten-nitrogen, nickel, cobalt-nickel-iron, iron, and manganese-iron.

49. The magnetic random access memory structure of claim 43, wherein said first magnetic layers have a pinned magnetic orientation.

50. The magnetic random access memory structure of claim 43, wherein said second magnetic layers have a free magnetic orientation.

51. The magnetic random access memory structure of claim 43, further comprising at least one second conductive line in contact with said at least one self-aligned contact.

52. A memory device comprising:

at least one magnetic random access memory cell, said magnetic random access memory cell comprising a first ferromagnetic layer formed over a first conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a second conductor in contact with a self-aligned contact, said self-aligned contact being a conductive layer included in said second ferromagnetic layer.

53. The memory device of claim 52, wherein said conductive layer is formed of tungsten nitrogen.

54. The memory device of claim 52, wherein said conductive layer is formed of tungsten.

55. The memory device of claim 52, wherein said first ferromagnetic layer has a pinned magnetic orientation.

56. The memory device of claim 52, wherein said second ferromagnetic layer has a free magnetic orientation.

57. A processor-based system, comprising:

a processor; and

an integrated circuit coupled to said processor, said integrated circuit including a plurality of magnetic random access memory cells, each of said magnetic random access memory cells including a first ferromagnetic layer formed over a first conductor, a second ferromagnetic layer formed over said first ferromagnetic layer, a nonmagnetic layer between said first and second ferromagnetic layers, and a second conductor in contact with a self-aligned contact, said self-aligned contact being a conductive layer included in said second ferromagnetic layers.

58. The processor-based system of claim 57, wherein said conductive layer is a tungsten nitrogen layer.

59. The processor-based system of claim 57, wherein said conductive layer is a tungsten layer.

60. The processor-based system of claim 57, wherein said first ferromagnetic layer has a pinned magnetic orientation.

61. The processor-based system of claim 57, wherein said second ferromagnetic layer has a free magnetic orientation.